Docket No.: 08211/0201750-US0
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Letters Patent of:
John Lee Barry et al.

Patent No.: 7,062,696

Issued: June 13, 2006

For: AN ALGORITHMIC TEST PATTERN GENERATOR, WITH BUILT IN SELF TEST (BIST) CAPABILITIES FOR FUNCTIONAL TESTING OF A CIRCUIT

REQUEST FOR CERTIFICATE OF CORRECTION
PURSUANT TO 37 CFR 1.323 AND PATENT OFFICE MISTAKE (37 CFR 1.322)

Attention: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Upon reviewing the above-identified patent, Patentee noted several patent office errors which should be corrected.

The following errors were not in the application as filed by applicant:

In the Specification:

Page 2, Col. 1 (Other Publications), Line 2, Delete "doucment" and insert -- document --.

Page 2, Col. 2 (Other Publications), Line 2, Delete "Singals" and insert -- Signals --.

Column 5, Line 4, Delete "assets" and insert -- asserts --.

Column 11, Line 51, In Claim 10, delete "20-bit" and insert -- 10-bit --.

Column 12, Line 8, In Claim 13, delete "patter" and insert -- pattern --.

Column 12, Line 60, In Claim 14, delete "sequence," and insert -- sequence; --.

Enclosed please find marked up copies of the List of References (1) page; Page 2 of the specification; Pages 4, 5 & 7 of the claims.

The following errors were found in the application as filed by applicant. The errors now sought to be corrected are inadvertent typographical errors. The correction of which does not involve new matter or require reexamination.

Sheet 4 of 18 (Fig. 2), Line 2 (Box 66), Delete "Algorithmmically" and insert - - Algorithmically - -.

Sheet 6 of 18 (Fig. 4A), Line 1 (Below Box 22), Delete "pattern-select_reg[3:0]" and insert - - pattern_select_reg[3:0] - -.

Column 7, Line 1, "five sample" and insert - - five-sample - -.

Column 11, Line 22, In Claim 6, delete "self test" and insert - - self-test - -.

Column 11, Line 25, In Claim 6, delete "self test" and insert - - self-test - -.

Column 13, Line 4, In Claim 14, delete "self test" and insert -- self-test --.

Column 13, Line 7, In Claim 14, delete "self test" and insert -- self-test --.

Transmitted herewith is a proposed Certificate of Correction effecting such amendment. Patentee respectfully solicits the granting of the requested Certificate of Correction.

The Commissioner is authorized to charge any deficiency of up to $300.00 or credit any excess in this fee to Deposit Account No. 04-0100. Payment of $100.00 is enclosed herewith.

Dated: September 14, 2006

Respectfully submitted,

By _____
Flynn Barrison
Registration No.: 53,970
DARBY & DARBY P.C.
P.O. Box 5257
New York, New York 10150-5257
(212) 527-7700
(212) 527-7701 (Fax)
Attorneys/Agents For Applicant

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO.	:	7,062,696
APPLICATION NO.	:	09/759,557
ISSUE DATE	:	June 13, 2006
INVENTOR(S)	:	John Lee Barry et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Specification:

Page 2, Col. 1 (Other Publications), Line 2, Delete "doucment" and insert

-- document --.

Page 2, Col. 2 (Other Publications), Line 2, Delete "Singals" and insert -- Signals --.

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MAILING ADDRESS OF SENDER (Please do not use customer number below):
Flynn Barrison
DARBY & DARBY P.C.
P.O. Box 5257
New York, New York 10150-5257

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MAILING ADDRESS OF SENDER (Please do not use customer number below):
Flynn Barrison
DARBY & DARBY P.C.
P.O. Box 5257
New York, New York 10150-5257

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Substitute for form **1449A/PTO**
(Modified by BSTZ 6/30/99)

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet	1	of	2

Complete if Known	
Application Number	New application
Filing Date	Herewith
First Named Inventor	John Lee BARRY
Group Art Unit	New application
Examiner Name	New application
Attorney Docket Number	04148.P013

U.S. PATENT DOCUMENTS

Examiner Initials *		U.S.Patent Document Number	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Filing Date if Appropriate
		4,503,536	Panzer	3/5/1985	9/13/1982
		4,974,184	Avra	11/27/1990	4/19/1990
		5,202,978	Nozuyama	4/13/1993	5/15/1989
		5,936,900	Hii, et al.	8/10/1999	11/14/1997

FOREIGN PATENT DOCUMENTS

Examiner Initials *		Foreign Patent Document Office or Country	Number	Date	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Translation? Yes/No

OTHER DOCUMENTS

Examiner Initials *		Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published (if known).	Translation? Yes/No
		Digital Visual Interface DVI, Revision 1.0, 02 April 1999, The Digital Display Working Group.	
		"Genlinx GS9022 Digital Video Serializer Data Sheet", Gennum Corporation, Revision August 1997, document no. 521-42-01.	
		SMPTE 259M - 1997: for Television - 10 Bit 4:2:2 Component and 4fsc NTSC Component Digital Signals - Serial digital Interface" Scopes of SMPTE Standards, 8/14/2000, http//www.smpte.org/stds/stscope.html.	

Examiner Signature		Date Considered	7/22/2003

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

AMENDMENTS TO THE SPECIFICATION

Please amendment paragraph [035] in the specification as follows:

[035] The method 70 commences at block 72 with the activation of the generator 10, for example by the assertion of an enable signal 90 illustrated in **Figure 1**. At block 74, where the generator 10 is capable of generating multiple patterns, a pattern to be generated by the generator 10 is selected utilizing, for example, the pattern select signal 14. As described above, the pattern select signal 14 provides input to the data input register block 12. At block 76, the pattern selection signal 14 is clocked through the buffer register 20 on a first clock signal. The pattern selection register 22 may store an indication of a previously selected pattern. The buffer register 20 and the pattern selection register 22 both provide input to the pattern change detector 24, thus allowing the detector 24 to detect a change in pattern selection. Responsive to a detection of a change in pattern selection, the pattern change detector 24 asserts a change pattern signal 26, which then operates to reset to the pattern generation state machine 30.

a plurality of logic gates that are operable to select one of two values associated with reading from the equalizer pathological table based on a line count value and the pattern selection value.

130. (Previously presented) The circuit of Claim 121, wherein each table in the memory component is organized as a plurality of five-sample segments; each of the five-sample segments includes four 10-bit data samples, and further includes a repeat field having a repeat value that indicates how many times the four 10-bit data samples are to be repeated; for each of the plurality of data samples that each include a unique data word, the repeat field has a value of one; and wherein for each of the five-sample segments other than the plurality of samples that each include a unique data word, the repeat field has a value greater than ten.

131. (Previously presented) The circuit of Claim 130, wherein the memory component further includes:

a line index table that stores values indicating a number of lines to transmit before switching to and from vertical blanking lines to active video lines.

132. (Previously presented) The circuit of Claim 131, further comprising:

a line counter that is operable to track a number of lines transmitted, and to compare the number of lines transmitted against values in the line index table to determine when to switch to and from vertical blanking lines and active video lines;

a sample counter; and

a repeat counter, wherein the repeat counter is employed in control of the repeating of each of the four 10-bit data samples a number of times indicated by the repeat value.

133. (Currently amended) A circuit for testing that is capable of creating any of a plurality of creatable digital video test patterns, comprising:

a pattern generation state machine that is operable to control a sequencing of a creation of a digital video test pattern selected for creation among the plurality of creatable digital video test patterns; and

a memory component that is operable to provide a table output value based on the control of the sequencing, wherein the memory component includes:

a header table that stores:

a plurality of data samples that each include a unique data word; and

a sequence of data that includes a portion of a repeating horizontal blanking data sequence for horizontal blanking lines, and further includes a repeat field that indicates a number of repetitions for the repeating horizontal blanking sequence.

134. (Currently amended) The circuit of Claim 133, further comprising:

an output register that is operable to create the digital ~~component~~ video test pattern selected for creation based on the table output value.

135. (Currently amended) A circuit for testing that is capable of creating any of a plurality of creatable video test patterns, comprising:

a pattern generation state machine that is operable to control a sequencing of a creation of a video test pattern selected for creation among the plurality of creatable video test pattern; and

a memory component that is operable to provide a table output value based on the control of the sequencing, wherein the memory component includes:

a header table that stores:

a plurality of data samples that each include a unique data word; and

a sequence of data that includes a portion of a repeating horizontal blanking data sequence, and further includes a repeat field that indicates a number of repetitions for the repeating horizontal blanking sequence; and~~The circuit of Claim 133, further comprising:~~

a pattern selection register that is operable to store and provide a pattern selection value, wherein the pattern selection value indicates which of the plurality of creatable video test patterns has been selected for creation.

136. (Currently amended) A circuit for testing that is capable of creating any of a plurality of creatable video test patterns, comprising:

plurality of at least sixteen creatable component video test patterns is, when created, a complete television video picture suitable for testing of digital television video processing equipment;

a pattern generation state machine that is operable to control a sequencing of a creation of the component video test pattern selected for creation by providing a plurality of clear and increment signals;

a memory component that is operable to provide a table output value based on the plurality of clear and increment signals and the pattern selection value, wherein the table output value is provided by tracking a location in a data sequence based on the clear and increment signals, and wherein the memory component includes:

a line index table that stores values indicating a number of lines to transmit before switching to and from vertical blanking lines to active video lines; and

a header table that stores:

a plurality of forty-bit data samples that each include a unique ten-bit data word; and

a sequence of data that includes a portion of a repeating horizontal blanking data sequence ~~for the horizontal blanking lines~~, and further includes a repeat field that indicates a number of repetitions for the repeating horizontal blanking sequence;

a colour table;

a PLL pathological table; and

an equalizer pathological table;

a plurality of logic gates that are operable to select one of two values associated with reading from the equalizer pathological table based on a line count value and the pattern selection value;

an output register that is operable to create the component video test pattern selected for creation based on the table output value;

a built-in self test circuit that stores, for each of the plurality of at least sixteen creatable component video test patterns, a pre-calculated expected checksum, wherein the built-in self test circuit is operable to perform actions, including:

determining a checksum for the created component video test pattern output by the output register; and